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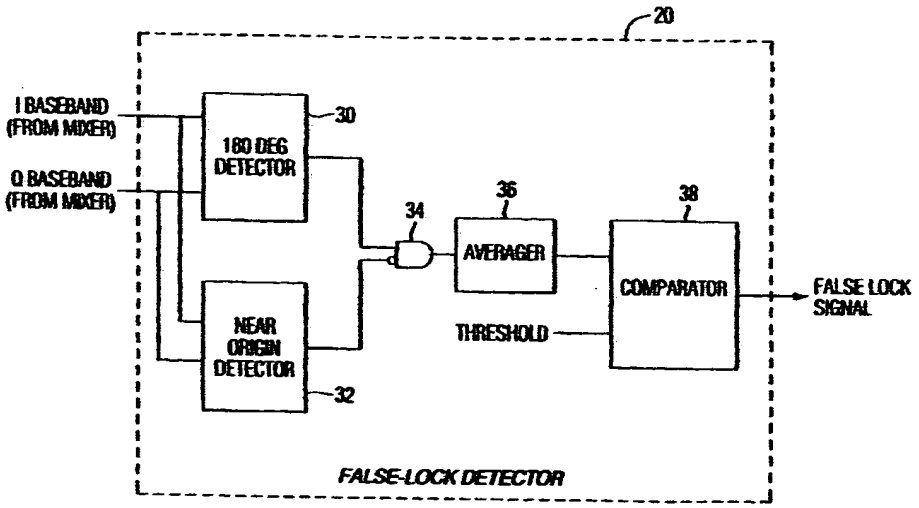
(54) Title: DEVICE AND METHODS FOR FALSE CARRIER LOCK DETECTION IN A RECEIVER



(57) Abstract: A receiver includes a demodulator and a false carrier lock detector circuit for a quadrature amplitude modulated (QAM) signal. The demodulator includes a controllable oscillator and an offset frequency generator for generating an offset frequency for the controllable oscillator to lock to a carrier of the QAM signal. The demodulator is susceptible to false carrier locking responsive to the offset frequency being substantially equal to the symbol rate divided by four or an integer multiple thereof. The receiver further includes the false carrier lock detector circuit including a first detector for detecting consecutive symbols spaced 180° apart, and a second detector for determining whether an intervening sample between the consecutive symbols is outside a predetermined distance from the origin.

WO 01/01650 A1

DEVICE AND METHODS FOR FALSE CARRIER LOCK DETECTION IN A RECEIVER

The present invention relates to the field of communications, and, more particularly, to radio communications using quadrature amplitude modulation (QAM) signals.

Quadrature amplitude modulation (QAM) is widely used for digital data transmission over radio links. With the applications in inter-active technologies such as Digital TV and the Internet, QAM as a communications technology, will continue to be integrated into consumer electronic devices. Indeed, high definition television (HDTV) signals will be transmitted as compressed digitized data using QAM. QAM transmits data as a sequence of two-dimensional complex symbols, i.e. with both in-phase and quadrature components. Each symbol adopts a specific pre-defined value based upon the data it represents. A set of all of the values available for transmission defines a character set which forms a constellation, when graphically plotted on a two-dimensional basis.

The size and shape of the constellation depends upon the number of discrete values in the set and their spatial location in the constellation. The constellation proposed for use in broadcasting HDTV data contains, e.g., 16, 32 or 64 values.

To receive a QAM signal, a QAM demodulator within a receiver performs the functions of timing recovery, equalization and carrier recovery. Carrier recovery creates a reference carrier for determination of in-phase (i) and quadrature modulated (q) components, both in terms of frequency and phase, such that the received demodulated symbols do not rotate when the carrier is locked. It is the carrier signal that is quadrature modulated by the symbols and then transmitted to the receiver. Carrier recovery must be able to properly function in the presence of varying frequency offsets, drift and/or jitter that often occurs between a QAM transmitter and the receiver.

Through carrier recovery, a carrier frequency offset value is typically translated into a direct current (DC) value or digitized value that is used as a control input to a voltage or numerically controlled oscillator within a phase-locked loop. The output of this oscillator, being locked in frequency and phase to the reference carrier signal, is then used to extract, for example, baseband quadrature modulated information from the received signal.

In a QAM demodulator, a circuit is used to detect that the demodulator is locked, i.e., that the carrier and clock recovery loops are synchronized. This circuit is

often called an Eye Quality Monitor ("EQM"). If it detects that the demodulator is unlocked, then the demodulator enters the acquisition mode and the carrier recovery circuit searches for the right carrier frequency, for example, by the use of a sweep circuit.

A carrier recovery circuit for a QAM demodulator is disclosed in the specifications of U.S. Patent No. 5,471,508. The carrier recovery circuit is operated in two modes: an acquisition mode to first attain an initial carrier lock, during which reduced constellation slicing is used; and a tracking (or lock) mode, during which full slicing is used to accurately track variations in frequency and phase that may occur to the carrier while the circuit remains locked.

Detecting the constellation size of a QAM signal is disclosed in the specifications of U.S. Patent No. 5,381,450. The probability density function of a received QAM signal is analyzed to determine the constellation size, e.g., 4, 16, 32, etc.

A problem can arise with the standard algorithms in that if the voltage controlled oscillator ("VCO") in the carrier recovery circuit oscillates with an offset frequency of exactly $R_S/4$ (R_S is the Symbol Rate), or a multiple of $R_S/4$, the demodulator would be erroneously declared locked. This is called a false-lock condition. It can occur when the symbol rate of the system is low, so that $R_S/4$ is inside the locking range of the carrier recovery.

A conventional way to perform the EQM function is to examine the received constellation (FIG. 1). The received signal is sampled once per symbol at the optimum sampling instant, and if there are too many non-valid symbols during a certain period, the demodulator is declared unlocked. If the VCO in the carrier recovery oscillates with an offset of exactly $R_S/4$, then the constellation rotates at $R_S/4$. Accordingly, between each sample, it moves by exactly one quadrant and the received symbols are declared valid.

The present invention includes a receiver for a quadrature amplitude modulated (QAM) signal comprising a demodulator for generating, from the QAM signal, received symbols about an origin at a symbol rate, said demodulator comprising a controllable oscillator and an offset frequency generator for generating an offset frequency for said controllable oscillator to lock to a carrier of the QAM signal, characterized in that said demodulator being susceptible to false carrier locking responsive to the offset frequency being substantially equal to the symbol rate divided by four or an integer multiple there of and a false carrier lock circuit comprising a first detector for detecting consecutive symbols

spaced 180° apart, and a second detector cooperating with said first detector for determining false carrier locking further based upon an intervening sample between the consecutive symbols being outside a predetermined distance from the origin.

The invention also includes a method for detecting false carrier locking of a demodulator for a quadrature amplitude modulated (QAM) signal, the method characterized by the steps of:

generating, from the QAM signal, received symbols about an origin at a symbol rate;

generating an offset frequency for a controllable oscillator of the demodulator to lock to a carrier of the QAM signal, the demodulator being susceptible to false carrier locking responsive to the offset frequency being substantially equal to the symbol rate divided by four or a multiple thereof;

detecting whether consecutive received symbols are spaced 180° apart;

detecting whether an intervening sample between the consecutive received symbols is outside a predetermined distance from the origin; and determining false carrier locking based upon the consecutive received symbols being 180° apart and the intervening sample being outside the predetermined distance from the origin.

An object of the invention to provide accurate carrier recovery for a QAM signal, and to increase the reliability of a QAM demodulator circuit by detecting a false-lock condition.

Advantageously, a receiver for a quadrature amplitude modulated (QAM) signal comprising a demodulator for generating, from the QAM signal, received symbols about an origin at a symbol rate. The demodulator comprises a controllable oscillator and an offset frequency generator for generating an offset frequency for the controllable oscillator to lock to a carrier of the QAM signal. The demodulator is susceptible to false carrier locking responsive to the offset frequency being substantially equal to the symbol rate divided by four or a multiple thereof.

Conveniently, the receiver further includes a false carrier lock circuit comprising a first detector for detecting consecutive symbols spaced 180° apart, and a second detector cooperating with the first detector for determining false carrier locking further based upon an intervening sample between the consecutive symbols being outside a predetermined distance from the origin. Thus, the receiver can determine a false carrier lock condition and re-initialize the carrier locking operation.

The false carrier lock circuit may comprise an output circuit for generating a false-lock signal responsive to the first and second detectors. Such an output circuit preferably

includes at least one logic gate connected to outputs of the first and second detectors, an averager for receiving pulses from the at least one logic gate, and a comparator for comparing an output of the averager to a threshold to generate the false-lock signal.

Additionally, the second detector preferably processes samples at twice the symbol rate. Also, the controllable oscillator and offset frequency generator define a locking frequency range so that for relatively low symbol rates, the symbol rate divided by four is within the locking frequency range. The demodulator may include a timing recovery circuit, and the receiver may include a tuner, an analog-digital converter connected between the tuner and the demodulator, and a decoder connected to the demodulator.

According to a method aspect of the invention, steps are provided for detecting false carrier locking of a demodulator for a quadrature amplitude modulated (QAM) signal. The steps include generating, from the QAM signal, received symbols about an origin at a symbol rate, and generating an offset frequency for a controllable oscillator of the demodulator to lock to a carrier of the QAM signal. The demodulator is susceptible to false carrier locking responsive to the offset frequency being substantially equal to the symbol rate divided by four or a multiple thereof. Further, the method includes: detecting whether consecutive received symbols are spaced 180° apart; detecting whether an intervening sample between the consecutive received symbols is outside a predetermined distance from the origin; and determining false carrier locking based upon the consecutive received symbols being 180° apart and the intervening sample being outside the predetermined distance from the origin.

The invention will now be described by way of example, with reference to the accompanying drawings in which:

FIG. 1 is a constellation plot illustrating the prior art method of monitoring the received QAM signal.

FIG. 2 is a simplified schematic diagram of a receiver including a false carrier lock detector.

FIG. 3 is a more detailed schematic diagram of a false carrier lock detector as shown in FIG 2; and

FIGS. 4 and 5 are constellation plots illustrating the method.

The invention is directed to a false carrier lock detector for a QAM demodulator circuit and associated methods which detect that the constellation rotates at $R_s/4$ (or a multiple of $R_s/4$) and that the QAM demodulator circuit is falsely locked. The basic components of a receiver 10 including a false carrier lock detector in accordance with the

present invention will now be described with reference to FIGS. 2 and 3. The receiver 10 includes a tuner 12 and an analog-digital converter 14 for initial processing of a received QAM signal. The receiver 10 also includes a demodulator 16 and a decoder 18 for subsequent processing and outputting of the information of the received QAM signal.

The demodulator 16 generates, from the QAM signal, received symbols about an origin at a symbol rate. A typical demodulator 16 includes a carrier recovery circuit 22 and a timing recovery circuit 24. As is conventional, the timing circuit 24 generates clock pulses to ensure that sampling occurs at a predetermined rate, e.g. the symbol rate. Furthermore, the carrier recovery circuit 22 performs carrier recovery through a phase-locked loop (PLL) in which a reference carrier is generated for use in de-rotating incoming symbols.

The carrier recovery circuit 22 includes a controllable oscillator 26, such as a voltage controlled oscillator (VCO), and an offset frequency generator 28 for generating an offset frequency for the controllable oscillator 26 to lock to a carrier of the QAM signal. Unfortunately, the demodulator 16 is susceptible to false carrier locking responsive to the offset frequency being substantially equal to the symbol rate (R_s) divided by four ($R_s/4$), or an integer multiple thereof. The controllable oscillator 26 and offset frequency generator 28 define a locking frequency range. The false carrier locking can occur when the symbol rate is relatively low, so that $R_s/4$ is within the locking frequency range.

Therefore, the receiver 10 includes a false carrier lock detector 20 to detect a false-lock condition of the demodulator 16. The false carrier lock detector 20 of the invention samples the constellation at twice the symbol rate. In the normal case, when the constellation is not rotating, if two consecutive received symbols are 180° apart, the sample taken between the two symbols will be close to the origin. This is shown in FIG. 4, where A and C indicate the two consecutive symbols, and X represents the intervening sample which is illustratively inside the window W around the origin. When the constellation is rotating at $R_s/4$ or an integer multiple thereof, however, if two consecutive received symbols A' and B' are 180° apart, the intervening sample X' taken between the two symbols will not be close to the origin, as shown in FIG. 5. Instead the intervening sample X' will be outside the window W.

Referring again more particularly to FIG. 3, in the false carrier lock detector 20, the I and Q baseband signals coming from the demodulator 16 are applied to a 180° detector circuit 30 that detects that two consecutive symbols are 180° apart.

Also, the I and Q baseband signals are applied to a second or near origin detector circuit 32 that detects whether n intervening sample is inside a window around the origin. If two consecutive symbols A' and B' are 180° apart and the intervening sample X' is not close to the origin (FIG. 5), a pulse is presented at the output of a logic gate 34, for example,

an AND gate with an inverted input coupled to the near origin detector 32. Those pulses are counted or integrated over a predetermined time by an averaging circuit or averager 36. If the output of the averager 36 is higher than a predetermined threshold, a false-lock condition is indicated as an output at the output of the averager 36 comparator circuit 38.

The averager 36 and the comparator 38 can be either digital or analog, and the averager may include an RC lowpass filter. The false lock detector 20 of the present invention can be used for any QAM modulation, e.g., 4, 16, 32, 64, 128, or 256 QAM.

According to a method aspect of the invention, steps are provided for detecting false carrier locking of the demodulator 16. The steps include generating, from the QAM signal, received symbols about an origin at a symbol rate, and generating an offset frequency for a controllable oscillator 26 of the demodulator 16 to lock to a carrier of the QAM signal. As discussed above, the demodulator 16 is unfortunately susceptible to false carrier locking responsive to the offset frequency being substantially equal to $R_s/4$ or an integer thereof.

Also, the method includes the step of processing samples at twice the symbol rate. Further, the method includes: detecting whether consecutive received symbols are spaced 180° apart; detecting whether an intervening sample between the consecutive received symbols is outside a predetermined distance from the origin; and determining false carrier locking based upon the consecutive received symbols A' and B' being 180° apart and the intervening sample X' being outside the predetermined distance an window W' from the origin, as illustrated in FIG. 5.

The method may include the step of generating a false-lock signal based upon the false carrier locking determination. Referring to FIG. 3, generating this false-lock signal preferably includes the steps of: generating pulses based upon the consecutive received symbols being 180° apart and the intervening sample being outside the predetermined distance from the origin; generating an average of the pulses over a predetermined time; and comparing the average with a threshold to generate the false-lock signal.

The receiver 10 including the false locking detector circuit 20 and can be used for a wide range of radio frequency ranges, and is particularly beneficial for microwave radio frequencies.

A receiver includes a demodulator and a false carrier lock detector circuit for a quadrature amplitude modulated (QAM) signal. The demodulator includes a controllable oscillator and an offset frequency generator for generating an offset frequency for the controllable oscillator to lock to a carrier of the QAM signal. The demodulator is susceptible to false carrier locking responsive to the offset frequency being substantially equal to the symbol rate divided by four or an integer multiple thereof. The receiver further includes the

false carrier lock detector circuit including a first detector for detecting consecutive symbols spaced 180° apart, and a second detector for determining whether an intervening sample between the consecutive symbols is outside a predetermined distance from the origin.

CLAIMS:

1. A receiver for a quadrature amplitude modulated (QAM) signal comprising a demodulator for generating, from the QAM signal, received symbols about an origin at a symbol rate, said demodulator comprising a controllable oscillator and an offset frequency generator for generating an offset frequency for said controllable oscillator to lock to a carrier of the QAM signal, characterized in that said demodulator being susceptible to false carrier locking responsive to the offset frequency being substantially equal to the symbol rate divided by four or an integer multiple there of and a false carrier lock circuit comprising a first detector for detecting consecutive symbols spaced 180° apart, and a second detector cooperating with said first detector for determining false carrier locking further based upon an intervening sample between the consecutive symbols being outside a predetermined distance from the origin.

2. A receiver as claimed in Claim 1 characterized in that said false carrier lock circuit comprises an output circuit for generating a false lock signal responsive to said first and second detectors, in which said output circuit comprises at least one logic gate connected to outputs of said first and second detectors, an averager for receiving pulses from said at least one logic gate, and a comparator for comparing an output of said averager to a threshold to generate the false lock signal, and said second detector processes samples at twice the symbol rate.

3. A receiver as claimed in Claim 1 characterized in that said controllable oscillator and offset frequency generator define a locking frequency range so that for relatively low symbol rates, the symbol rate divided by four is within the locking frequency range, and said demodulator further comprises a timing recovery circuit.

4. A receiver as claimed in Claim 1 characterized in that a tuner an analog-digital converter connected between said tuner and said demodulator; and a decoder connected to said demodulator.

5. A receiver for a quadrature amplitude modulated (QAM) signal comprising a demodulator for generating, from the QAM signal, received symbols about an origin at a symbol rate, characterized in that a false carrier lock circuit comprising a first detector for detecting consecutive symbols spaced 180° apart, and a second detector cooperating with said first detector for determining false carrier locking of said demodulator further based upon an intervening sample between the consecutive symbols being outside a predetermined distance from the origin, in which said false carrier lock circuit comprises a output circuit for generating a false lock signal responsive to said first and second detectors.

6. A receiver as claimed in to Claim 5 characterized in that said output circuit

comprises at least one logic gate connected to outputs of said first and second detectors, an averager for receiving pulses from said at least one logic gate, and a comparator for comparing an output of said averager to a threshold to generate the false lock signal.

7. A receiver as claimed in to Claim 5 characterized in that said demodulator comprises a controllable oscillator and an offset frequency generator for generating an offset frequency for said controllable oscillator to lock to a carrier of the QAM signal; and wherein said controllable oscillator and offset frequency generator define a locking frequency range so that for relatively low symbol rates, the symbol rate divided by four is within the locking frequency range.

8. A false carrier lock circuit for a quadrature amplitude modulated (QAM) signal comprising a first detector for detecting consecutive received symbols of the QAM signal being 180° spaced apart, a second detector for determining whether an intervening sample between the consecutive received symbols is outside a predetermined distance from an origin, characterized in that said first and second detectors cooperating to detect false carrier locking based upon the consecutive received symbols being 180° apart and the intervening sample being outside the predetermined distance from the origin, including an output circuit for generating a false lock signal responsive to said first and second detector.

9. A receiver including a false carrier lock circuit as claimed in Claim 8 characterized in that said output circuit comprises, at least one logic gate connected to outputs of said first and second detectors, an averager for receiving pulses from said at least one logic gate, a comparator for comparing an output of said averager to a threshold to generate the false lock signal, in which said second detector processes samples at twice the symbol rate, said first detector and said near origin detector each receive I and Q baseband signals generated from the QAM signal.

10. A method for detecting false carrier locking of a demodulator for a quadrature amplitude modulated (QAM) signal, the method characterized by the steps of:

generating, from the QAM signal, received symbols about an origin at a symbol rate;

generating an offset frequency for a controllable oscillator of the demodulator to lock to a carrier of the QAM signal, the demodulator being susceptible to false carrier locking responsive to the offset frequency being substantially equal to the symbol rate divided by four or a multiple thereof;

detecting whether consecutive received symbols are spaced 180° apart;

detecting whether an intervening sample between the consecutive received symbols is outside a predetermined distance from the origin; and determining false carrier

locking based upon the consecutive received symbols being 180° apart and the intervening sample being outside the predetermined distance from the origin.

11. A method as claimed in Claim 10 characterized by the step of generating a false lock signal based upon the false carrier locking determination, in which the step of generating a false lock signal comprises the steps of generating pulses based upon the consecutive received symbols being 180° apart and the intervening sample being outside the predetermined distance from the origin, generating an average of the pulses over a predetermined time, comparing the average with a threshold to generate the false lock signal, and including the step of sampling the symbols at twice the symbol rate.

12. A method for detecting false carrier locking for a quadrature amplitude modulated (QAM) signal, the method characterized by the steps of detecting whether consecutive received symbols of the QAM signal are spaced 180° apart, detecting whether an intervening sample between the consecutive received symbols is outside a predetermined distance from an origin, determining false carrier locking based upon the consecutive received symbols being 180° apart and the intervening sample being outside the predetermined distance from the origin, including the step of generating a false lock signal based upon the false carrier locking determination.

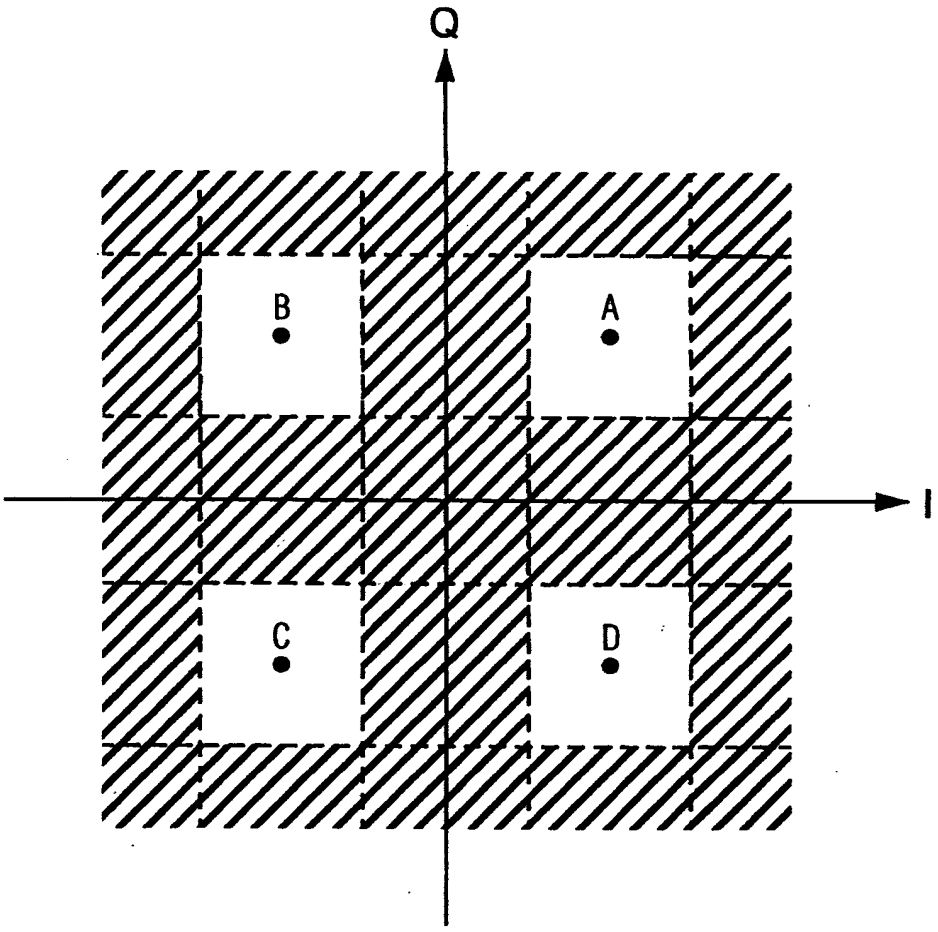


FIG. 1
PRIOR ART

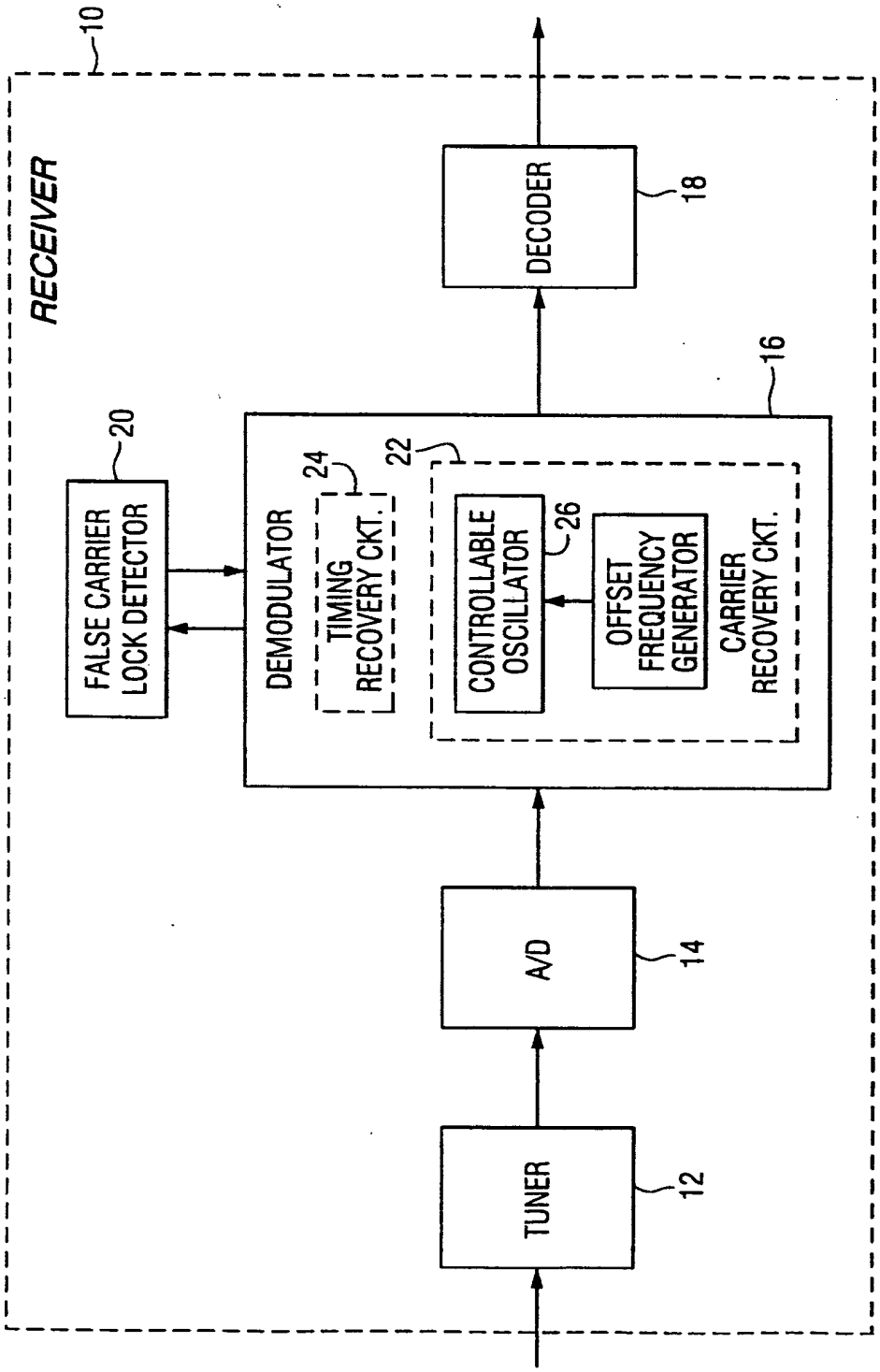

10
RECEIVER
DECODER
18
16
20
22
24
FALSE CARRIER LOCK DETECTOR
DEMODULATOR
TIMING RECOVERY CKT.
CONTROLLABLE OSCILLATOR
26
OFFSET FREQUENCY GENERATOR
CARRIER RECOVERY CKT.
A/D
14
TUNER
12

FIG. 2

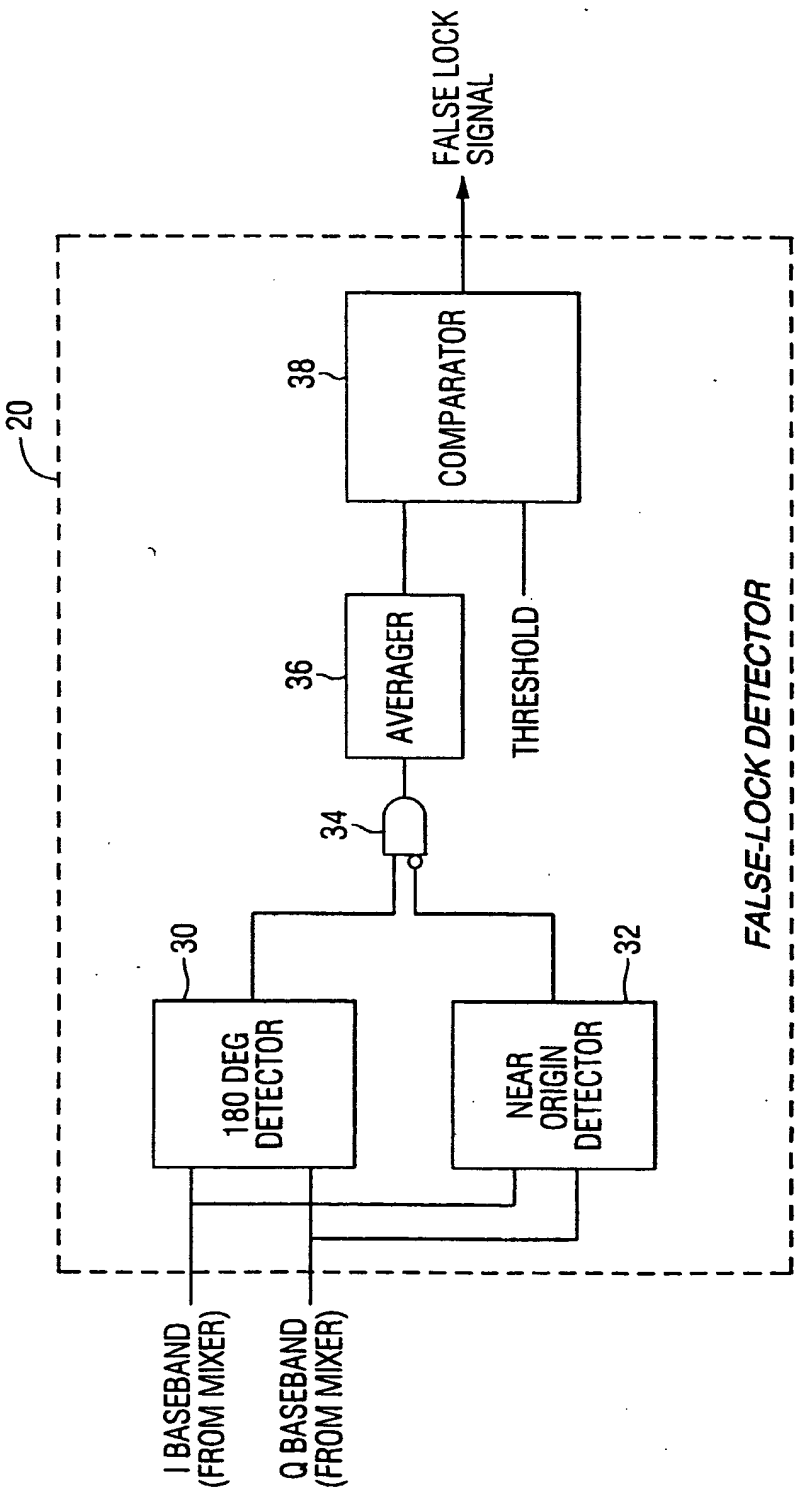

FALSE LOCK SIGNAL
20
38
COMPARATOR
36
AVERAGER
THRESHOLD
34
30
180 DEG DETECTOR
32
NEAR ORIGIN DETECTOR
FALSE-LOCK DETECTOR
I BASEBAND (FROM MIXER)
Q BASEBAND (FROM MIXER)

FIG. 3

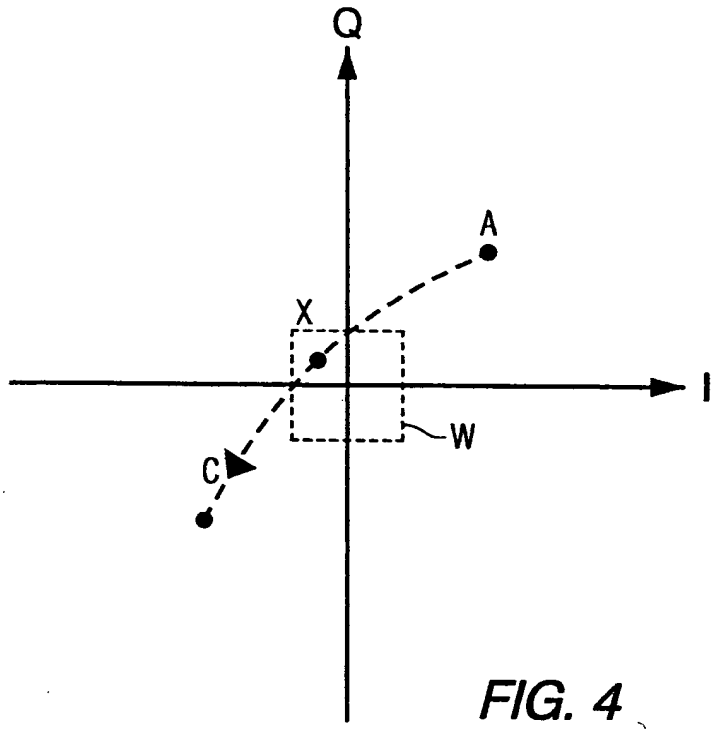


FIG. 4

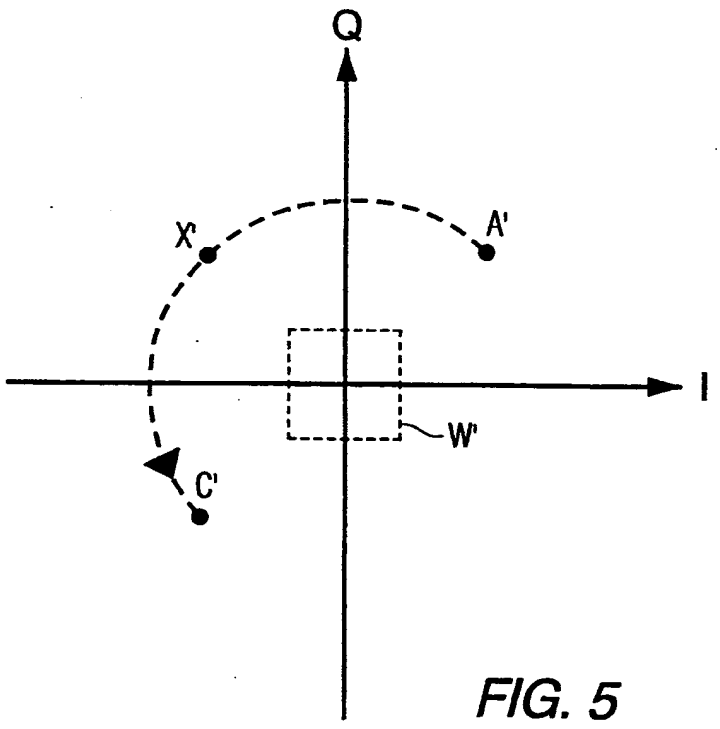


FIG. 5

INTERNATIONAL SEARCH REPORT

Int. ional Application No
PCT/US 00/18103

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04L27/38

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, INSPEC, COMPENDEX, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4 079 329 A (ENGLAND JON D ET AL) 14 March 1978 (1978-03-14) column 8, line 40 - line 62	1-12
A	EP 0 768 783 A (LORAL AEROSPACE CORP) 16 April 1997 (1997-04-16) column 2, line 57 -column 3, line 13	1-12
A	SAITO Y ET AL: "256 QAM MODEM FOR HIGH CAPACITY DIGITAL RADIO SYSTEM" IEEE TRANSACTIONS ON COMMUNICATIONS, vol. COM-34, no. 8, August 1986 (1986-08), pages 799-805, XP000758524 New York, USA ISSN: 0090-6778 page 804, left-hand column	1-12

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

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Date of the actual completion of the international search	Date of mailing of the international search report
30 October 2000	07/11/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Orozco Roura, C

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Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter onal Application No
PCT/US 00/18103

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